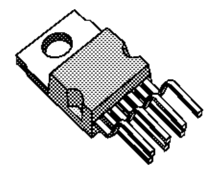
L4923

5V–1A VERY LOW DROP REGULATOR WITH RESET AND INHIBIT

- VERY LOW DROP (max. 0.9V at 1A) OVER FULL OPERATING TEMPERATURE RANGE (– 40 / + 125 °C)
- LOW QUIESCENT CURRENT (max 70 mA at 1 A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SETTABLE DELAY
- INHIBIT FOR REMOTE ON-OFF COMMAND (active high)
- LOAD STANDBY CURRENT
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



Heptawatt

ORDERING NUMBER : L4923

DESCRIPTION

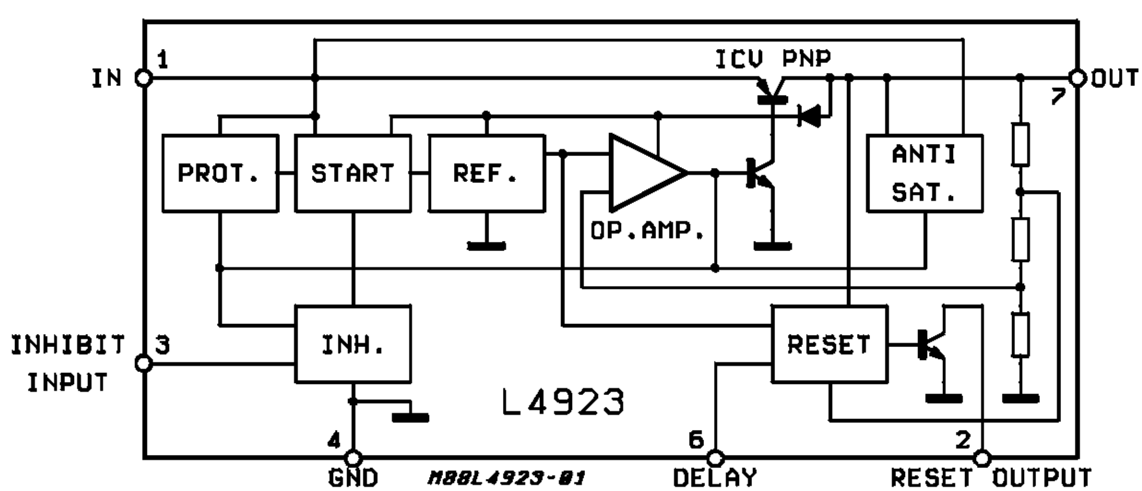
The L4923 is a high current monolithic voltage regulator with very low voltage drop (0.70 V max at 1 A, T_J = 25 °C).

The device is internally protected against load dumps transient of + 60 V, input overvoltage, reverse polarity, overheating and output short circuit : thanks to these features the L4923 is very suited for the automotive and industrial applications.

The reset function is very useful for power off and power on information when supplying a microprocessor.

The inhibit function reduces drastically the consumption when no load current is required : typically the standby current value is 300 µA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
V_r	DC Reverse Voltage	– 18	V
V_D	Positive Load Dump Protection (t = 300ms)	60	V
T_J	Junction Temperature range	– 40 to 150	°C
T_{op}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction Case	4	°C/W

PIN CONNECTION

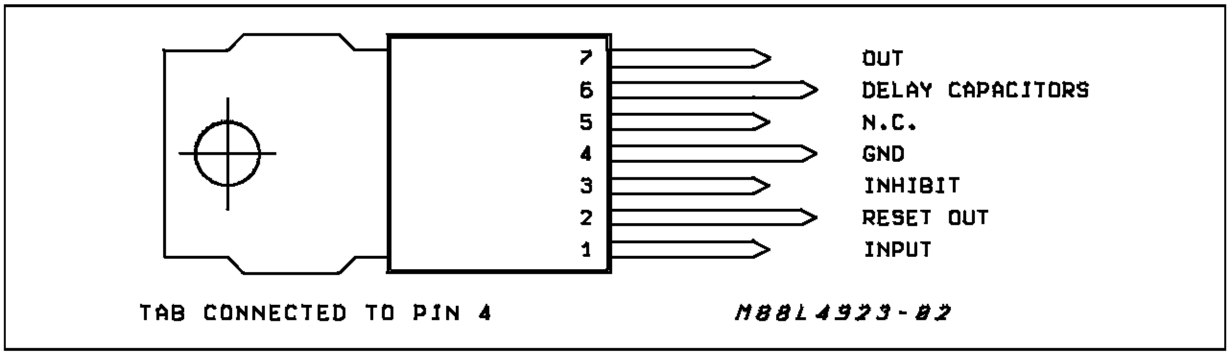
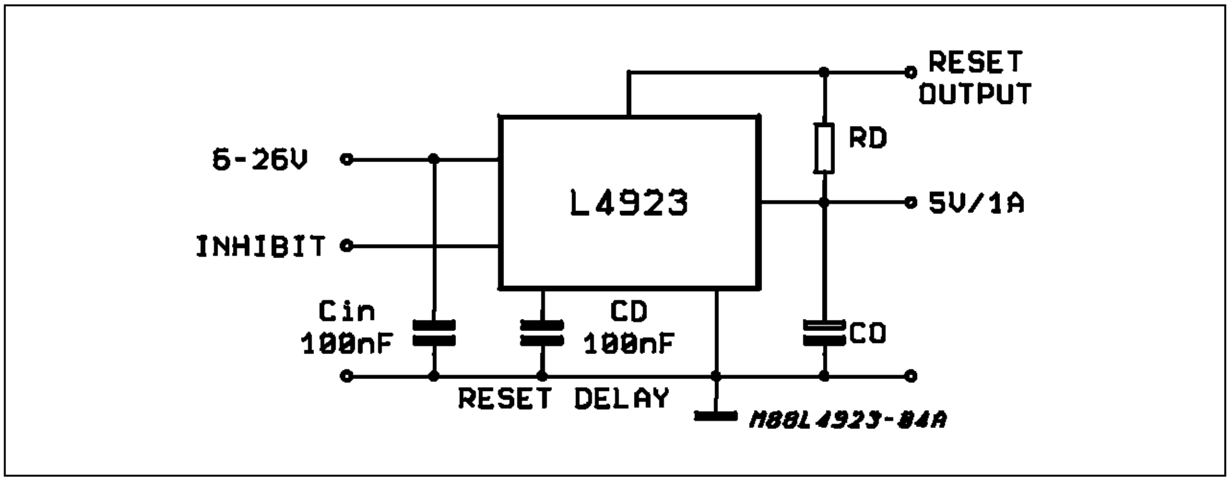


Figure 1 : Application Circuit.



(*) RECOMMENDED VALUE : C_0 = 47 µF, ESR < 10 Ω, (I_{out} > 10 mA) OVER FULL T_{range}.

ELECTRICAL CHARACTERISTICS (V_i = 14. 4V, – 40°C ≤ T_J ≤ + 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	(*) Note 1	6		26	V
V_o	Output Voltage	I_o = 0mA to 1A T_J = 25°C	4.8 4.9		5.2 5.1	V V
ΔV_{Line}	Line Regulation	V_i = 6 to 26V; I_O = 10mA		5	25	mV
SVR	Supply Voltage Rejection	I_o = 700mA f = 120Hz; C_o = 47µF V_i = 12V_{dc} + 5V_{pp}		55		dB
ΔV_{LOAD}	Load Regulation	I_o = 10mA to 1A		15	50	mV
$V_i - V_o$	Dropout Voltage	T_J = 25°C, I_O = 1A		0.45	0.70	V
		Over Full T, I_o = 1A			0.90	V
I_q	Quiescent Current	I_o = 10mA I_o = 1A Active High Inhibit		7 25 0.30	12 70 0.65	mA mA mA
I_{SC}	Short Circuit Current			1.8		A
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± 5V_{pp}	50	60		dB
V_R	Rset Output Saturation Voltage	1.5V < V_O < $V_{RT\,(off)}$, I_R = 1.6mA 3V < V_O < $V_{RT\,(off)}$, I_R = 8mA			0.40 0.40	V V
$V_{RT\,peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_O		0.65	1.0	V
I_R	Reset Output Leakage Current (high level)	V_o in Regul. V_R = 5V			50	µA
t_D	Reset Pulse Delay Time	C_D = 100nF		20		ms
V_{RthOFF}	Power OFF V_o Threshold	V_o @ Reset out H to L Transition; T_J = 25°C – 40°C ≤ T_J ≤ + 125°C	 4.75 4.7	 V_o – 0.15		 V V
I_{C6}	Delay Capacitor Charging Current (current generator)	V_6 = 3V		20		µA
V_{RthON}	Power ON V_o Threshold	V_o @ Reset out L to H Transition		V_{rthOFF} + 0.03V	V_o – 0.04V	V
V_6	Delay Comparator Threshold	Reset out = "1" H to L Transition	3.2		3.8	V
		Reset out = "0" L to H Transition	3.7	4	4.4	V
V_{6H}	Delay Comparator Hysteresis			500		mV
V_{InhL}	Low Inhibit Voltage				0.5	V
V_{InhH}	High Inhibit Voltage		2.0			V
I_{InhL}	Low Level Inhibit Current	$V_{Inh\,L}$ = 0.4V	– 40	– 10		µA
I_{InhH}	High Level Inhibit Current	$V_{Inh\,H}$ = 2.4V		6	20	µA

(*) Note 1 : The device is not operating within the range : 26 V < V_i < 37 V.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor wich can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450 mV) and low quiescent current (I_Q = 20 mA typically at I_O = 1 A).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

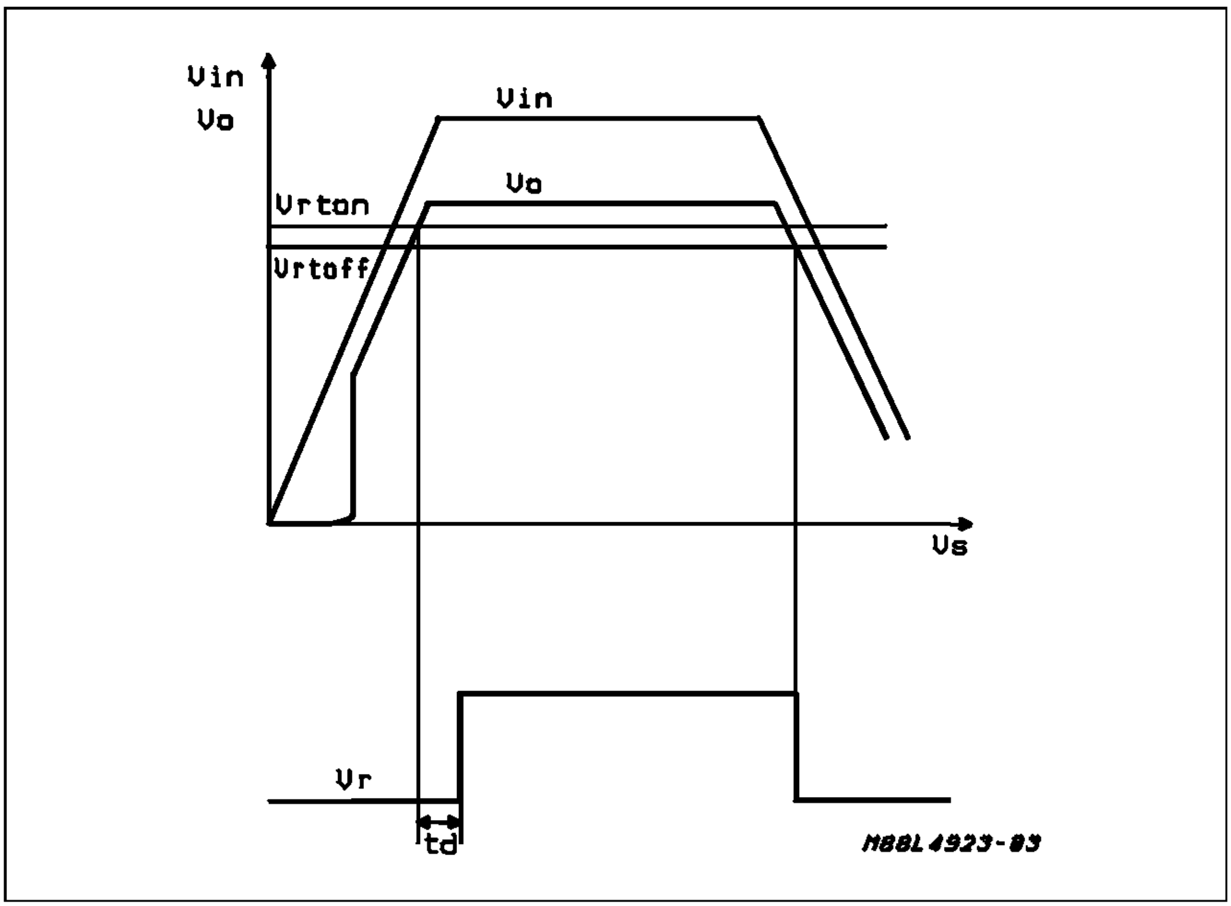
The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{Omin} = 22 µF) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the current peak which takes place during the start up.

The reset function is LOW active when the output voltage level is lower than the reset threshold voltage V_{Rth} (typ. value : V_O - 150 mV). When the output voltage is higher than V_{Rth} the reset becomes HIGH after a delay time settable with the external capacitor C_d. Typically t_d = 20 ms, C_d = 0.1 µF. The reset threshold hysteresis improves the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 2.

The inhibit circuit accepts standard TTL input levels : this block switches off the voltage regulator when the input signal is HIGH and switches on it when the input signal is LOW. Thanks to inhibit function the consumption is drastically reduced (650 µA max) when no load current is required.

Figure 2 : Typical Reset Output Waveform.



HEPTAVATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

